What is claimed is:

1. A fabrication method for multiple LCD panel models from transistor array substrates formed on a common substrate, the method comprising the steps of:

selecting areas on the common substrate where switching array substrates of different sizes will be formed;

fabricating switching devices using a common set of masks for each of the switching array substrates;

forming an alignment layer on each of the transistor array substrates;

forming a seal pattern around each of the transistor array substrates;

scattering spacers onto each transistor array substrate;

attaching the common substrate on which the switching devices are formed to a color filter substrate to form an LCD display panel;

cutting the LCD display panel into individual LCD panel models;

injecting liquid crystal into each of the panel models through a liquid crystal injecting hole; and

sealing the liquid crystal injecting hole.

2. The method of claim 1, wherein the switching devices are thin film transistors.

3. The method of claim 1, wherein the step of fabricating comprises the step of fabricating through a four mask process that includes a diffraction slit mask.

4. The method of claim 3, wherein the slit mask includes a 'U'-shaped

channel slit-pattern.

5. The method of claim 3, wherein the slit mask comprises a 'U'-shaped source forming pattern, a bar-shaped drain forming pattern, and a channel slit-pattern between the source forming pattern and the drain forming pattern.

6. The method of claim 1, wherein the step of fabricating switching devices comprises:

forming a gate electrode on the common substrate;

forming a gate insulating layer;

forming an active layer on the gate insulating layer;

forming source and drain electrodes on the active layer;

forming a passivation layer on the common substrate; and

forming pixel electrodes connected to the drain electrodes.

7. A fabrication method for multiple transistor array substrates on a common substrate for multiple LCD panel models, the method comprising the steps of:

selecting areas on the common substrate where switching array substrates of different sizes will be formed;

fabricating the switching devices for each switching array substrate, regardless of size, through a multiple-mask process that applies the same masks for each switching array substrate.

8. The method of claim 7, where the step of forming the switching devices comprises the steps of:

fabricating gate lines on each switching array substrate;

forming a gate insulating layer for insulating the gate lines;

forming an active layer on the gate insulating layer;

forming source and drain electrodes on the active layer;

forming a passivation layer on the common substrate; and

forming a pixel electrode on the passivation layer.

9. The method of claim 7, where the switching device is a thin film transistor.

10. A method for fabricating transistor array substrates on a common glass substrate, the method comprising the steps of:

selecting a first area on the common substrate for a first transistor array substrate of a first size;

selecting a second area on the common substrate for a second transistor array substrate of a second size;

depositing a conductive layer and a photoresist layer on the first and second transistor array substrates;

exposing the photoresist layer above transistor channel areas for the first and second transistor array substrates through a transistor channel diffraction slit;

etching completely through the photoresist layer in at least one location in each of the first and second transistor array substrates, while removing less than all of the photoresist layer exposed through the diffraction slit, thereby leaving thinner regions in the photoresist layer above the transistor channel areas;

removing the thinner regions in the photoresist layer; and

etching through the conductive layer above the transistor channel areas to

form source electrodes and drain electrodes.

11. The method of claim 10, further comprising the steps of:

forming contact holes to expose a portion of the drain electrodes; and

forming pixel electrodes connected through the contact holes to the drain electrodes.

12. The method of claim 10, further comprising the step of fabricating gate electrodes with a first mask.

13. The method of claim 12, wherein the step of exposing the photoresist layer comprises the step of exposing the photoresist layer with a second mask.

14. The method of claim 11, further comprising the step of fabricating gate electrodes with a first mask, and where:

the step of exposing the photoresist layer comprises the step of exposing the photoresist layer through a second mask comprising the diffraction slit;

the step of forming contact holes employs a third mask; and

the step of forming the pixel electrodes employs a fourth mask.

15. A method for forming switching transistors for an LCD transistor array substrate, the method comprising the steps of:

employing a first mask during a first photolithography process to form gate lines on a first transistor array substrate and a second transistor array substrate, the first and second transistor array substrates different in size;

employing a second mask during a second photolithography process for diffraction exposure of a photoresist layer above transistor channel areas for the first and second transistor array substrates, and where the second photolithography process includes the step of etching completely through the photoresist layer in at least one location in each of the first and second transistor array substrates, while etching less than all of the photoresist layer above the transistor channel areas, thereby leaving step-down regions in the photoresist layer above the transistor channel areas;

removing the step-down regions in the photoresist layer to expose a conductive layer; and

etching the conductive layer above the transistor channel areas to form source and drain electrodes in the conductive layer.

16. The method of claim 15, where the step of removing comprises ashing.

17. The method of claim 15, where the second mask comprises a diffraction slit.

18. The method of claim 15, where the second mask defines a 'U'-shaped transistor.

19. The method of claim 15, where the removing step further comprises the step of maintaining at least a portion of the photoresist layer above the source and drain electrodes.

20. The method of claim 15, further comprising the step of etching an active layer between the source and drain electrodes.